March 26, 2001

TO: Commissioner of Patents and Trademarks
Washington, D.C. 20231

FROM: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

SUBJECT: **Continuation of:**

Serial #:	09/351,237
File Date:	7/12/99
Inventor:	Yi, X., et al.
Examiner:	
Art Unit:	
Title:	Gap Filling Process in Integrated Circuit using Low Dielectric Constant Materials

PRELIMINARY AMENDMENT

Please enter the following Preliminary Amendment for the above referenced

Continuation Application:

EXPRESS MAIL CERTIFICATE

Express Mail No. EF230880448 US
I Hereby Certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed to: The Commissioner of Patents and Trademarks, Washington, DC 20231. **Applicant and/or Attorney requests the date of deposit as the Filing Date.**

March 26, 2001
Date of Deposit

Signature / Date March 26, 2001

PLEASE AMEND THE SPECIFICATION AS FOLLOWS:

After the title, please insert the following new paragraph:

"This application is a Continuation of serial number 09/351,237, filed on July 12, 1999, issued as US Patent 6, 207, 554, and assigned to a common assignee".

PLEASE AMEND THE CLAIMS AS FOLLOWS:

Please cancel Claims 2-22.

PLEASE ENTER THE FOLLOWING NEW CLAIMS:

23. A method for fabricating multilevel metal interconnections having low dielectric constant insulators on a substrate comprising the steps of:

providing first metal lines, formed over said substrate;

coating a layer of low dielectric constant insulating material on and in between said metal lines;

curing the low dielectric constant material;

depositing a thin layer of an adhesion promoter and stabilizing material on the low dielectric constant material;

depositing a silicon oxide cap layer on the adhesion promoter and over the low

dielectric constant material; and

planarizing the silicon oxide cap layer by chemical mechanical polish (CMP).

24 The method of claim 23, wherein said low dielectric constant material is spun on dielectric, deposited to a thickness of about 4,000 to 12,000 Angstroms, with curing conditions at 400^0C for 1 hr., in a nitrogen ambient gas flow from about 1 to 30 SLM, oxygen less than 10 ppm.

25. The method of claim 23, wherein said layer of adhesion promoter and stabilizer is a non-oxide compound.

26. The method of claim 25, wherein said layer of adhesion promoter and stabilizer is silicon nitride, deposited by plasma enhanced chemical vapor deposition to a thickness of between about 200 and 500 Angstroms.

27. The method of claim 23, wherein said silicon oxide cap layer is deposited by plasma enhanced chemical vapor deposition, to a thickness of between about 4,000 to 16,000 Angstroms.

28. A method for fabricating multilevel metal interconnections having low dielectric constant insulators on a substrate comprising the steps of:

providing first metal lines, formed over said substrate, said metal lines having a top hard mask layer;

coating a layer of low dielectric constant insulating material on and in between said first metal lines;

curing the low dielectric constant material;

chemically mechanically polishing back and planarizing the surface of said low dielectric constant material to the level of said top hard mask layer;

depositing a second layer of low dielectric material over said first layer of low dielectric constant material and over said metal lines;

curing the second layer of low dielectric constant material; and

depositing a second hard mask layer over the second low dielectric constant layer.

29. The method of claim 28, wherein said top hard mask layer comprises silicon nitride and silicon oxide, wherein said silicon oxide is deposited by plasma enhanced chemical vapor deposition to a thickness of between about 200 and 500 Angstroms, and said silicon nitride is deposited to a thickness of between about 1,000 and 2,000 Angstroms.

30. The method of claim 28, wherein said first low dielectric constant material is spun on dielectric, and is deposited by spin coating to a thickness of between about 4,000 and 12,000 Angstroms, and cured at about 400^0C, for about 1 hr., in N_2 gas flow of 1 to 30 SLM, and in O_2 of less than about 10 ppm.

31. The method of claim 28, wherein said chemical mechanical polishing conditions are: polishing rate 1,000 to 2,500 A/mm, platen speed of 20 to 80 rpm, carry speed of 20 to 80 rpm, downward force 2 to 8 psi, backside pressure from 1 to 7 psi.

32. The method of claim 28, wherein said second low dielectric constant material is a spun on dielectric, deposited by spin coating to a thickness of about 4,000 to 12,000 Angstroms, with curing conditions of 400^0C, 1 hr., in N_2 gas at a flow rate of about 1 to 30 SLM, and in O_2 of less than about 10 ppm.

33. The method of claim 28, wherein said second hard mask layer comprises silicon nitride and silicon oxide deposited by plasma enhanced chemical vapor deposition, to a thickness of about 200 to 500 Angstroms of silicon nitride and to a thickness of about 1,000 to 2,000 Angstroms of silicon oxide.

34. The method of claim 28, wherein said top hard mask layer is selected from the group consisting of silicon nitride and silicon oxide, solely silicon nitride, or solely silicon oxide.

35. The method of claim 28, wherein said second hard mask layer is selected from the group consisting of silicon nitride and silicon oxide, solely silicon nitride, or solely silicon oxide.

36. A method for fabricating multilevel metal interconnections having low dielectric constant insulators on a substrate comprising the steps of:

providing first metal lines, formed over said substrate, said metal lines having a dielectric anti-reflective layer thereover, and a top hard mask layer over said dielectric anti-reflective layer;

coating a layer of low dielectric constant insulating material on and in between said first metal lines;

curing the low dielectric constant material;

chemically mechanically polishing back and planarizing the surface of said low dielectric constant material to the level of said top hard mask layer;

depositing a layer of adhesion promoter over the top hard mask layer and over said low dielectric constant insulating material; and

depositing a silicon oxide cap layer on the adhesion promoter layer.

37. The method of claim 36, wherein said top hard mask layer comprises silicon nitride and silicon oxide deposited by plasma enhanced chemical vapor deposition, to a thickness of about 200 to 500 Angstroms of silicon nitride and to a thickness of about 1,000 to 2,000 Angstroms of silicon oxide.

38. The method of claim 36, wherein said top hard mask layer is selected from the group consisting of silicon nitride and silicon oxide, solely silicon nitride, or solely silicon oxide.

39. The method of claim 36, wherein said low dielectric constant material is low dielectric constant spun on dielectric, deposited by spin coating to a thickness of about 4,000 to 12,000 Angstroms, with curing conditions of 400^0C, 1 hr., in N_2 gas flow 1 to 30 SLM, and in O_2 of less than 10 ppm.

40. The method of claim 36, wherein said layer of adhesion promoter and stabilizer is silicon nitride deposited by plasma enhanced chemical vapor deposition in a thickness range from about 200 to 500 Angstroms.

41. The method of claim 36, wherein said layer of cap oxide is silicon oxide deposited by plasma enhanced chemical vapor deposition, to a thickness range from about 4,000 to 12,000 Angstroms.

REMARKS

Please enter the above Preliminary Amendment in the above referenced Continuation Application. All claims are believed to be in allowable condition. Please also accept the attached Terminal Disclaimer, and the associated fee.

The Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

It is requested that should there be any problems with this Amendment, please call the undersigned Attorney at (845) 452-5863.

Respectfully submitted,

Stephen B. Ackerman, Reg. No, 37,761

VERSION WITH MARKINGS TO SHOW CHANGES MADE

PLEASE AMEND THE SPECIFICATION AS FOLLOWS:

After the title, please insert the following new paragraph:

"This application is a Continuation of serial number 09/351,237, filed on July 12, 1999, issued as US Patent 6, 207, 554, and assigned to a common assignee".

PLEASE AMEND THE CLAIMS AS FOLLOWS:

Please cancel Claims 2-22.

PLEASE ENTER THE FOLLOWING NEW CLAIMS:

23. A method for fabricating multilevel metal interconnections having low dielectric constant insulators on a substrate comprising the steps of:

providing first metal lines, formed over said substrate;

coating a layer of low dielectric constant insulating material on and in between said metal lines;

curing the low dielectric constant material;

depositing a thin layer of an adhesion promoter and stabilizing material on the low dielectric constant material;

depositing a silicon oxide cap layer on the adhesion promoter and over the low dielectric constant material; and

planarizing the silicon oxide cap layer by chemical mechanical polish (CMP).

24 The method of claim 23, wherein said low dielectric constant material is spun on dielectric, deposited to a thickness of about 4,000 to 12,000 Angstroms, with curing conditions at 400^0C for 1 hr., in a nitrogen ambient gas flow from about 1 to 30 SLM, oxygen less than 10 ppm.

25. The method of claim 23, wherein said layer of adhesion promoter and stabilizer is a non-oxide compound.

26. The method of claim 25, wherein said layer of adhesion promoter and stabilizer is silicon nitride, deposited by plasma enhanced chemical vapor deposition to a thickness of between about 200 and 500 Angstroms.

27. The method of claim 23, wherein said silicon oxide cap layer is deposited by plasma enhanced chemical vapor deposition, to a thickness of between about 4,000 to 16,000 Angstroms.

28. A method for fabricating multilevel metal interconnections having low dielectric constant insulators on a substrate comprising the steps of:

providing first metal lines, formed over said substrate, said metal lines having a top hard mask layer;

coating a layer of low dielectric constant insulating material on and in between said first metal lines;

curing the low dielectric constant material;

chemically mechanically polishing back and planarizing the surface of said low dielectric constant material to the level of said top hard mask layer;

depositing a second layer of low dielectric material over said first layer of low dielectric constant material and over said metal lines;

curing the second layer of low dielectric constant material; and

depositing a second hard mask layer over the second low dielectric constant layer.

29. The method of claim 28, wherein said top hard mask layer comprises silicon nitride and silicon oxide, wherein said silicon oxide is deposited by plasma enhanced chemical vapor deposition to a thickness of between about 200 and 500 Angstroms, and said silicon nitride is deposited to a thickness of between about 1,000 and 2,000

Angstroms.

30. The method of claim 28, wherein said first low dielectric constant material is spun on dielectric, and is deposited by spin coating to a thickness of between about 4,000 and 12,000 Angstroms, and cured at about 400^0C, for about 1 hr., in N_2 gas flow of 1 to 30 SLM, and in O_2 of less than about 10 ppm.

31. The method of claim 28, wherein said chemical mechanical polishing conditions are: polishing rate 1,000 to 2,500 A/mm, platen speed of 20 to 80 rpm, carry speed of 20 to 80 rpm, downward force 2 to 8 psi, backside pressure from 1 to 7 psi.

32. The method of claim 28, wherein said second low dielectric constant material is a spun on dielectric, deposited by spin coating to a thickness of about 4,000 to 12,000 Angstroms, with curing conditions of 400^0C, 1 hr., in N_2 gas at a flow rate of about 1 to 30 SLM, and in O_2 of less than about 10 ppm.

33. The method of claim 28, wherein said second hard mask layer comprises silicon nitride and silicon oxide deposited by plasma enhanced chemical vapor deposition, to a thickness of about 200 to 500 Angstroms of silicon nitride and to a thickness of about 1,000 to 2,000 Angstroms of silicon oxide.

34. The method of claim 28, wherein said top hard mask layer is selected from the group consisting of silicon nitride and silicon oxide, solely silicon nitride, or solely silicon

oxide.

35. The method of claim 28, wherein said second hard mask layer is selected from the group consisting of silicon nitride and silicon oxide, solely silicon nitride, or solely silicon oxide.

36. A method for fabricating multilevel metal interconnections having low dielectric constant insulators on a substrate comprising the steps of:

providing first metal lines, formed over said substrate, said metal lines having a dielectric anti-reflective layer thereover, and a top hard mask layer over said dielectric anti-reflective layer;

coating a layer of low dielectric constant insulating material on and in between said first metal lines;

curing the low dielectric constant material;

chemically mechanically polishing back and planarizing the surface of said low dielectric constant material to the level of said top hard mask layer;

depositing a layer of adhesion promoter over the top hard mask layer and over said low dielectric constant insulating material; and

depositing a silicon oxide cap layer on the adhesion promoter layer.

37. The method of claim 36, wherein said top hard mask layer comprises silicon nitride and silicon oxide deposited by plasma enhanced chemical vapor deposition, to a thickness of about 200 to 500 Angstroms of silicon nitride and to a thickness of about 1,000 to 2,000 Angstroms of silicon oxide.

38. The method of claim 36, wherein said top hard mask layer is selected from the group consisting of silicon nitride and silicon oxide, solely silicon nitride, or solely silicon oxide.

39. The method of claim 36, wherein said low dielectric constant material is low dielectric constant spun on dielectric, deposited by spin coating to a thickness of about 4,000 to 12,000 Angstroms, with curing conditions of 400^0C, 1 hr., in N_2 gas flow 1 to 30 SLM, and in O_2 of less than 10 ppm.

40. The method of claim 36, wherein said layer of adhesion promoter and stabilizer is silicon nitride deposited by plasma enhanced chemical vapor deposition in a thickness range from about 200 to 500 Angstroms.

41. The method of claim 36, wherein said layer of cap oxide is silicon oxide deposited by plasma enhanced chemical vapor deposition, to a thickness range from

about 4,000 to 12,000 Angstroms.